IN THE SPECIFICATION:

Please amend the paragraph on page 4, line 20 to page 5, line 11, entitled "Chiplet Process" to read as follows:

Referring now to the Figures of the drawing, the chiplet process begins with fabricating the silicon device chiplet wafer 12 through the semiconductor device and bottom wiring layers 13 and the top metal wiring level 14, application of the final passivation dielectric stack 16, and the opening of the terminal pad vias (TV) 19. The TV via openings 19 can be as small as 2.5 microns in width and the passivation layer is about 1 micron or less in thickness. Then the following steps are carried out: Deposit by sputtering or other vacuum deposition methods a liner layer 15, which typically comprises about ~~400A~~ 400Å tantalum nitride (TaN) and ~~400A~~ 400Å Tantalum(Ta) and a seed layer 17, comprising about ~~1000A~~ 1000Å or more of vacuum deposited copper. Other liner materials that can be used include Ti, TiN, W, WN and Cr among others. The wafer is then subjected to chemical-mechanical polishing (CMP) so as to polish the copper from the top surface of the wafer stopping on the Ta surface. This results in a structure as shown in Figure 1 wherein the copper seed 17 is preserved only at the bottom and the side walls of the TV openings 19. Electroplate a barrier layer 20, which can be Ni, Co, Pt, Pd and the like of about ~~5000A~~ 5000Å thickness followed by a joining metal layer 22, which is a fusible solder such as 97% Pb 3% Sn alloy, Au-Sn alloys or other solders depending upon the application and solder hierarchy desired. Pb free solders based on Sn and its alloys are also possible for layer 22. The solder layer thickness can be chosen to be between 2 microns to 100 microns depending on the solder alloy and the application need. The key feature to note is that layers 20 and 22 plate up only on the Cu present in the TV openings 19 and not on the liner layer 15 present on the top of the wafer. The liner layer 15 serves simply as an electrode to carry the plating current in the process. Layer 15 is subsequently removed by dry plasma or wet

chemical etching from the chiplet top surface regions between the contact pads leaving behind a residual TaN Ta layer 15', only in the TV via bottom and side walls of the chiplet pad structure as shown in Figure 3 (bottom).

The paragraph on page 5, line 21 to page 6, line 8, was amended to read as follows:

The subsequent process flow for the carrier wafers has the following steps: Deposit by sputtering or other vacuum deposition methods a liner layer 39, which typically comprises about ~~400A~~ 400Å tantalum nitride (TaN) and ~~400A~~ 400Å Tantalum (Ta) and a seed layer 40, comprising about ~~1000A~~ 1000Å of vacuum deposited copper. The wafer is then subjected to chemical-mechanical polishing (CMP) so as to polish the copper from the top surface of the wafer stopping on the Ta surface. This results in a structure on the carrier as shown in Figure 2 wherein the copper seed 40, is preserved only at the bottom and the side walls of the TV openings 38. Electroplate a barrier layer 41, which can be Ni, Co, Pt, Pd and the like of about ~~5000A~~ 5000Å thickness followed by a noble metal layer 42, which is preferably gold in the thickness range of 1000 to ~~10,000A~~ 1000Å to 10,000Å. The key feature to note is that layers 41 and 42 plate up only on the Cu present in the TV openings 38, and not on the liner layer present on the top surface of the carrier wafer. The liner layer 39, serves simply as an electrode to carry the plating current in the process. Layer 39 is subsequently removed by dry plasma or wet chemical etching from the top surface regions between the pads leaving behind a residual TaN Ta layer 39, only in the TV via bottom and side walls of the carrier pad structure as shown in Figure 3 (top). Other methods for applying the barrier layer 41 and noble metal layer 42 include electroless deposition. Electroless deposition of Ni, Co, Pd as well as noble metal Au is known in the art and can be used instead of electroplating. Electroless Au plating and immersion Au are particularly suitable if thin Au ~~(about 800 to 1200A)~~ (about 800Å to 12,000Å) is deemed sufficient.

The resulting feature on the carrier is receptacle 44 for receiving microjoints fabricated on the chiplet.

The following paragraph was inserted at the end of the section on page 5 entitled "chiplet Process" and before the end of the section entitled "Carrier Process:"

Preferably, the liner layer thickness in the system according to the present invention is between 50Å and 1200Å. Also preferably, the seed layer in the system according to the present invention is copper with thickness in the range 300Å to 2000Å. More preferably, the seed layer in the system according to the present invention is copper with thickness in the range 300Å to 2000Å, and the microjoint pads on the device chips include successive layers of a liner layer, seed layer, barrier layer and a fusible solder layer, respectively.